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PTO IDENTIFIER: **Application Number** 10/697,012-Conf. #8254
Patent Number

Inventor: Eric Adler et al.

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FROM: CONNOLLY BOVE LODGE & HUTZ LLP
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Attorney Dkt. #: 21806-00070-US1

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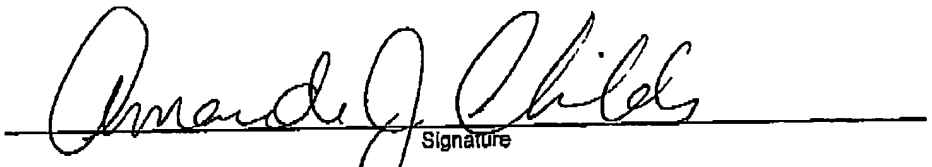

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FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/697,012-Conf. #8254
Filing Date	October 31, 2003
First Named Inventor	Eric Adler
Examiner Name	Not Yet Assigned
Art Unit	N/A
Attorney Docket No.	21806-00070-US1

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 09-0456 Deposit Account Name: IBM Corporation (Burlington)

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
8	-20=	x	=

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
3	-3=	x	=

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
- 100 =	/50	(round up to a whole number) x	=	

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal	500.00

SUBMITTED BY					
Signature	Myron Keith Wyche	Registration No. (Attorney/Agent)	47,341	Telephone	(202) 331-7111
Name (Print/Type)	Myron Keith Wyche			Date	March 10, 2006

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Docket No.: 21806-00070-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Eric Adler et al.

Confirmation No.: 8254

Application No.: 10/697,012

Filed: October 31, 2003

Art Unit: 2812

For: SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE DEVICE HAVING AN ELECTRICALLY MODULATED CONDUCTION CHANNEL

Examiner: R. E. Pompey

APPEAL BRIEF

March 10, 2006

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is timely filed within two months of the Notice of Appeal filed in this case on January 10, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Arguments

451778

App. A Claims on Appeal
App. B Evidence
App. C Related Proceedings

I. REAL PARTY IN INTEREST

Real party in interest: International Business Machines Corporation, Burlington, VT USA.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application: There are 8 claims pending in this application.

B. Current Status of Claims

1. Claims canceled: 1-19
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 20-27
4. Claims allowed: None
5. Claims rejected: 20-27

C. Claims On Appeal: The claims on appeal are claims 20-27.

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Overview of Applicants' Claimed Invention

The present invention relates to the Metal Oxide Semiconductor (MOS) art. In particular, the present invention is a semiconductor device having an electrically modulated conduction

channel. The semiconductor device is located within a trench structure formed in a substrate of a MOS integrated circuit. The semiconductor device may be a Field Effect Transistor (FET) transistor, having a gate deposited over a diffusion region located within the trench structure. The diffusion region is electrically modulated by applying a control voltage to terminals connected to the trench structure and the substrate. In this way, the channel width below the gate can be modulated by the application of the control voltage, producing a change in the transistor gain. That is, the gain of the semiconductor device may effectively be set by varying the voltage potential. In addition, the trench structure may include multiple diffusion regions, each of which serve as a resistor controlled from a common control voltage applied to a gate electrode.

B. Detailed Summary of Claimed Invention with Reference to the Disclosure

A detailed discussion below is cross-referenced to the Specification and Figures is provided below as published in U.S. Patent Application Publication US 2004/0092109A1 (i.e., this application).

A transistor having an electrically modulated channel is shown in FIG. 1A through FIG. 1D of the application. In particular, FIG. 1A and FIG. 1B show a diffusion region **11** formed in an integrated circuit substrate **25** and surrounded by a trench **12**. In addition, FIG. 1A shows a gate **18** is formed over the diffusion region **11**. Source and drain regions are provided on either side of the gate **18** to form a transistor. A terminal connection **21** is formed on the trench **12**, to which a control voltage may be applied, and a similar terminal connection **22** is provided on the substrate **25**. The trench **12** is filled with a poly-silicon material **26** and includes a thin oxide layer **16** along the inner and outer side walls.

An electric field created between the trench 12 and integrated circuit substrate 25 modulates the channel width as shown in FIGS. 1C and 1D. In particular, as shown in FIG. 1A - FIG. 1D, trench terminal **21** and substrate terminal **22** are connected to trench **12** and integrated circuit substrate **25**, respectively. As shown in FIG. 1C, in response to the application of a positive voltage potential between terminal **21** and terminal **22**, a thin layer P= forms at the interface of the trench **12**. As a result, gate **18** will have a greater effective width than with no

voltage potential applied between trench terminal **21** and substrate terminal **22**. As shown in FIG. 1D, in response to the application of a negative voltage potential applied between trench terminal **21** and substrate terminal **22**, a thin layer P^+ forms at the interface of the trench **12**, effectively narrowing the width of the gate **18** and the channel width of the diffusion region underneath the gate **18**, when a voltage potential is applied between trench terminal **21** and substrate terminal **22**. In these ways, the channel width of the diffusion region is electrically modulated by the voltage potential applied between the trench terminal **21** and substrate terminal **22**. Therefore, "control over current flowing in said diffusion region," as recited in claims 20 and 26, is provided by applying a voltage potential between trench terminal **21** and substrate terminal **22**.

VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

A. 35 U.S.C. 102(b) rejection of claims 20-27 over US 5,241,210 (Nakagawa et al.)

B. 35 U.S.C. 102(e) rejection of claims 20-27 over US 6,118,152 (Yamaguchi et al.)

VII. ARGUMENT

Legal Principles

The Final Rejection includes rejections based on anticipation. "Anticipation under 35 USC §102(e) requires that 'each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.'" *In re Robertson*, 49 USPQ 1949, 1950 (Fed.Cir. 1999).

"[A]ll words in the claim must be considered in judging the patentability of the claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970). As set forth in section 2111 of the MPEP, "claims are interpreted in the broadest reasonable fashion *consistent with the specification.*" (Emphasis added). The Patent and Trademark Office *is required* to take into account whatever enlightenment is afforded by the

specification, *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ 2d 1023, 1027-28 (Fed. Cir. 1997). (Emphasis added).

- **§102(b) anticipation rejection of claims 20-27 in view of US 5,796,837 (Nakagawa et al.)**
- **§102(e) anticipation rejection of claims 20-27 in view of US 6,118,152 (Yamaguchi et al.)**

Accordingly, this Brief responds to the rejections of the claims on appeal as set forth in the explicit statements of the rejections as noted above.

1. The anticipation rejection over US 5,241,210 (Nakagawa et al.) is deficient, as the applied art does not disclose all the limitations of claims 20-27.

The Examiner asserts that Nakagawa et al. discloses all the claimed limitations. Appellants respectfully disagree, as discussed below.

As noted above, anticipation requires the disclosure, in a prior art reference, of each and every limitation as set forth in the claims.[1] There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. §102.[2] To properly anticipate a claim, the reference must teach every element of the claim.[3] "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference".[4] "The identical invention must be shown in as complete detail as is contained in the ...claim."[5] In determining anticipation, no claim

[1] *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985).
[2] *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (Fed. Cir. 1991).
[3] *See* MPEP § 2131.
[4] *Verdegaal Bros. v. Union Oil Co. of Calif.*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
[5] *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

limitation may be ignored.[6] The applied art of Nakagawa et al. does not meet this threshold burden.

Discussion of Nakagawa et al. and its deficiencies with regards to the claimed invention

Nakagawa et al. discloses a high breakdown voltage semiconductor device.[7] In particular, FIG. 6/FIG. 17 of Nakagawa et al. discloses a first semiconductor region **54/54a** isolated by oxide films **52/52a** and **53/53** formed on a substrate **51/51a**.[8] In addition, Nakagawa et al. discloses a fifth semiconductor region **59/59a** that is formed on a bottom portion of the first semiconductor region **54/54a** and contacting oxide film **52/52a**.[9] Further, Nakagawa et al. discloses first and second electrodes **62/62a, 63/63a** as source and drain electrodes, respectively, on layers **58/58a** and **57/57a** in a peripheral portion of the first semiconductor region **54/54a**.[10] Moreover, Nakagawa et al. discloses that the gate electrode **61/61a** is formed on a surface portion of a fourth semiconductor layer **57/57a**.

With regard to Nakagawa et al., the Office Action of August 10, 2005, states:

> Nakagawa discloses, in column 7, lines 26-32, that oxide 53/53a, see figures 6/17 respectively, forms a groove/trench and figure 17 *shows an electrode, clearly on section 64a,* which is filled into groove/trench 53/53a. Therefore, *the control electrodes are on the trench structure and read on the claims* (emphasis and punctuation added).[11]

In contrast to the "electrode clearly on section 64a," as indicated in the outstanding Office Action and disclosed by Nakagawa et al., the present invention claims, as recited in claim 20:

> forming electrical connections on said trench structure *and* said substrate which *receive a control voltage whereby an electric*

---

[6] *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 187 (Fed. Cir. 1990).
[7] Nakagawa et al. at ABSTRACT.
[8] *Id.* at FIG. 6; FIG. 17; column 7, lines 25-46; column 9, lines 36-49.
[9] *Id.* at FIG. 6; FIG. 17; column 7, lines 25-46; column 9, lines 36-49.
[10] *Id.* at FIG. 6; FIG. 17; column 7, lines 25-46; column 9, lines 36-49.
[11] Outstanding Office Action at page 4, paragraph, lines 4-7.

> *field is produced to control a current flowing in said diffusion region* (emphasis added);

and as recited in claim 26:

> forming multiple contacts on each of said trench structures *and* said substrate *for controlling current through said diffusion regions* (emphasis added).

That is, Applicants respectfully submit that Nakagawa et al. nowhere discloses a device with *both* a "trench structure" with a trench terminal connection **21** *and* "substrate" with substrate terminal connection **22**, as in the present invention; wherein "said *trench structure and said substrate* receive a control voltage whereby an electric field is produce to control a current flowing in said diffusion region," as recited in claims 20 and in similar language in claim 26.

In addition, it is respectfully submitted that the trench structure of Nakagawa et al. teaches away from that of the present invention. In particular, Nakagawa et al. teaches including an additional oxide film **52/52a** layer that is formed on top of the substrate **51a** at the bottom of the device. As recited in claims 20 and 27, "an electric field is produced to control current flowing in the diffusion region."

Thus, it is respectfully submitted that the oxide film **52/52a** formed on top of the substrate **51a**, as discussed above and disclosed by Nakagawa et al., would interfere with the formation of the electric field and negatively affect the operation of the invention, and in this way, Nakagawa et al. teaches away from the function of "controlling the current flowing in the diffusion region"

Therefore, it is respectfully submitted that Nakagawa et al. does not disclose, anticipate or inherently teach the claimed invention and that claims 20 and 26, and claims dependent thereon, patentably distinguish thereover.

2. The anticipation rejection over US 6,118,152 (Yamaguchi et al.) is deficient, as the applied art does not disclose all the limitations of claims 20-27.

The Examiner asserts that Yamaguchi et al. discloses all the claimed limitations. Appellants respectfully disagree, as discussed below.

Discussion of Yamaguchi et al. and its deficiencies with regards to the claimed invention

Yamaguchi et al. discloses a silicon layer provided in a silicon substrate through a buried oxide film that includes a silicon island partitioned by a trench.[12] In particular, Yamaguchi et al. discloses a silicon substrate **1**; a trench **5** surrounding a silicon island **8**; a silicon oxide film **6** for side walls formed on the trench **5**; and oxide films **13a, 13b** formed between a drain region **9** and well regions **10a, 10b**, respectively.[13] Further, Yamaguchi et al. discloses forming gate electrodes **15a, 15b** over the well regions **10a, 10b**.[14]

With regard to Yamaguchi et al., the Office Action mailed August 10, 2005, states:

> Yamaguchi discloses, in column 3, lines 42-48, that oxide 6 forms on the inside walls of trench 5 and *control electrode 19a/19b* are clearly on sections 7 which are filled into trench 5, see figure 1 and column 4, lines 24-53.[15]

In addition, the outstanding Office Action states: "the control electrode on the trench are electrodes 19a/19b."[16]

In contrast to the "electrodes 19a/19b," as indicated in the outstanding Office Action and disclosed by Yamaguchi et al., the present invention claims, as recited in claim 20:

> forming electrical connections on said trench structure *and* said substrate which *receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region* (emphasis added);

and as recited in claim 26:

> forming multiple contacts on each of said trench structures *and* said substrate *for controlling current through said diffusion regions* (emphasis added).

That is, Applicants respectfully submit that Yamaguchi et al. nowhere discloses a device with *both* a "trench structure" with a trench terminal connection **21** *and a* "substrate" with substrate

[12] Yamaguchi et al. at ABSTRACT.
[13] *Id.* at column 3, line 43 to column 4, line 53.
[14] *Id.* at column 3, line 43 to column 4, line 53.
[15] Outstanding Office Action at page 4, paragraph, lines 10-12.
[16] *Id.* at page 4, paragraph 4, lines 13-15.

terminal connection **22**, as in the present invention; wherein "said *trench structure and said substrate* receive a control voltage whereby an electric field is produce to control a current flowing in said diffusion region," as recited in claims 20 and in similar language in claim 26.

In addition, it is respectfully submitted that the trench structure of Yamaguchi et al. teaches away from that of the present invention. As shown in FIG. 1, Yamaguchi et al. teaches a trench structure **8** that surrounds *and includes* the gate electrodes **15a, 15b**.

In contrast, the present invention, as seen in FIG. 1A – FIG. 1D discloses a trench structure **16** that only partially encloses the gate structure **18**. In fact, as discussed above, a primary function of the present invention is the affect on the width of the diffusion channel **11** that the applied voltage potentials produce (i.e., the **P=** and **P+** layers) relative to the physical location of the trench structure **16** and the gate **18**. That is, along with the application of voltage potentials, the relative locations of the trench structure **16** and gate **18** are used to "control a current flowing in said diffusion region."

Thus, it is respectfully submitted that the position of the trench structure **8** and the gate electrodes **15b/15c**, as disclosed by Yamaguchi et al, would interfere and negatively affect the operation of the present invention. In this way, Yamaguchi et al. teaches away from the function of "controlling the current flowing in the diffusion region," as recited in claims 20 and 26.

Therefore, it is respectfully submitted that Yamaguchi et al. does not disclose, anticipate or inherently teach the claimed invention and that claims 20 and 26, and claims dependent thereon, patentably distinguish thereover.

VIII. CLAIMS

A copy of claims 20-27 involved in the present appeal is attached hereto as Appendix A.

Application No.: 10/697,012 Docket No.: 21806-00070-US1

In view of the Arguments presented above, reversal of the rejections by the Honorable Board and allowance of pending claims 20-27 is respectfully requested.

Respectfully submitted,

By_____
Myron Keith Wyche
Registration No.: 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
Agent for Applicant

APPENDIX A- CLAIMS ON APPEAL

Claims Involved in the Appeal of Application Serial No. 10/697,012

20. A method for making a semiconductor chip comprising:

forming a diffusion region in a semiconductor substrate;

forming an insulated trench structure in said substrate which surrounds said diffusion region; and

forming electrical connections on said trench structure and said substrate which receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region.

21. The method for making a semiconductor chip according to claim 20, further comprising source and drain regions formed in said diffusion on each side of a gate.

22. The method of making a semiconductor chip according to claim 20, wherein said diffusion region forms a resistor which has a resistance controlled in response to said control voltage.

23. The method of making a semiconductor chip according to claim 20, wherein said diffusion region is formed in a well of polysilicon deposited in said trench structure.

24. A method for making a semiconductor chip comprising:

forming first and second diffusion regions in a semiconductor substrate;

forming a trench structure around said first and second diffusion regions; and

forming a contact on said trench structure and said substrate for controlling current through said diffusion regions.

25. The method for making a semiconductor chip according to claim 24, further comprising:

forming first and second gates over said first and second diffusion regions.

26. A method for making a semiconductor chip comprising:

forming multiple diffusion regions that are surrounded by multiple trench structures on a substrate; and

forming multiple contacts on each of said trench structures and said substrate for controlling current through said diffusion regions.

27. The method for making a semiconductor chip according to claim 26, further comprising:

forming a gate electrode over each of said diffusion regions; and

forming drain and source connections on opposite sides of said gate electrodes.

APPENDIX B – EVIDENCE

NONE

Application No.: 10/697,012 Docket No.: 21806-00070-US1

APPENDIX C - RELATED PROCEEDINGS

NONE

Application No.: 10/697,012 Docket No.: 21806-00070-US1

In view of the Arguments presented above, reversal of the rejections by the Honorable Board and allowance of pending claims 20-27 is respectfully requested.

Respectfully submitted,

By Myron Keith Wyche
Myron Keith Wyche
Registration No.: 47,341
CONNOLLY BOVE LODGE & HUTZ LLP
Agent for Applicant

APPENDIX A- CLAIMS ON APPEAL

Claims Involved in the Appeal of Application Serial No. 10/697,012

20. A method for making a semiconductor chip comprising:

forming a diffusion region in a semiconductor substrate;

forming an insulated trench structure in said substrate which surrounds said diffusion region; and

forming electrical connections on said trench structure and said substrate which receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region.

21. The method for making a semiconductor chip according to claim 20, further comprising source and drain regions formed in said diffusion on each side of a gate.

22. The method of making a semiconductor chip according to claim 20, wherein said diffusion region forms a resistor which has a resistance controlled in response to said control voltage.

23. The method of making a semiconductor chip according to claim 20, wherein said diffusion region is formed in a well of polysilicon deposited in said trench structure.

24. A method for making a semiconductor chip comprising:

forming first and second diffusion regions in a semiconductor substrate;

forming a trench structure around said first and second diffusion regions; and

forming a contact on said trench structure and said substrate for controlling current through said diffusion regions.

25. The method for making a semiconductor chip according to claim 24, further comprising:

forming first and second gates over said first and second diffusion regions.

26. A method for making a semiconductor chip comprising:

forming multiple diffusion regions that are surrounded by multiple trench structures on a substrate; and

forming multiple contacts on each of said trench structures and said substrate for controlling current through said diffusion regions.

27. The method for making a semiconductor chip according to claim 26, further comprising:

forming a gate electrode over each of said diffusion regions; and

forming drain and source connections on opposite sides of said gate electrodes.

Application No.: 10/697,012 Docket No.: 21806-00070-US1

APPENDIX B – EVIDENCE

NONE

APPENDIX C - RELATED PROCEEDINGS

NONE